iSTART

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iSTART iReport

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iSTART-TEK Releases Its New Product, START™ v5, and Design Services

iSTART-TEK held a hybrid in-person and online event on March 25 to introduce its latest product, START™ v5, along with its design services. The event focused on detailed presentations of START™ v5 and EZ-BIST™ v2. START™ v5 is an EDA tool for SRAM testing and repair, while EZ-BIST™ v2 is an EDA tool specifically for SRAM testing. In terms of performance improvements, both START™ v5 and EZ-BIST™ v2 leverage AI tools, including ChatGPT, OpenAI, and DeepSeek, to enhance RTL syntax coverage and support for various commands. Compared to START™ v3, these enhancements boost execution efficiency by 50%.

Additionally, START™ v5 and EZ-BIST™ v2 significantly improve the efficiency of identifying various types of SRAM, reducing SRAM identification time by 50% compared to START™ v3. Furthermore, START™ v5 and EZ-BIST™ v2 have enhanced the Auto-Clock Tracing function for SRAM, allowing MCU-based chips to automatically identify SRAM clock paths within the chip, thereby improving the speed of SRAM circuit testing for MCU-based chips.

START™ v5 has obtained ISO 26262 TCL1 certification, with several features meeting the requirements for automotive electronic chips. The latest enhancements include the addition of a dynamic control interface for SRAM in the POT (Power-On Test) function. Instead of storing POT control commands in ROM, they are now stored in SRAM, allowing for dynamic adjustments to the POT control commands. SRAM repair technology has always been one of iSTART-TEK's proudest strengths.

Enhancements in START™ v5's SRAM repair technology include:

- Reduced latency in transferring SRAM error information from eFuse or OTP to the SRAM repair controller during the repair process.
- Introduced data compression for eFuse and OTP required in SRAM repair, addressing the increasing complexity of AI chip designs and the growing demand for SRAM. This significantly reduces AI chip costs.
- Optimized the timing of SRAM repair paths to accommodate the increasing SRAM demand in AI chips, enhancing overall flexibility in chip placement and routing.
- Enhanced the patented SRAM repair technology by strengthening the coexistence mechanism of Stand-Alone SRAM and Redundancy. This improvement gave consumer electronic chip designs more flexibility, allowing unused SRAM space to be fully utilized as backup memory for repair, significantly reducing design costs for consumer chips.
- Strengthened the modular (Bottom-Up) design workflow to support the Chiplet architecture, simplifying the generation of SRAM testing and repair circuits for complex chips. Additionally, ensured compliance with SRAM testing standards under the Chiplet architecture.

In terms of SRAM error diagnosis, START™ v5 and EZ-BIST™ v2 have enhanced SRAM error analysis capabilities, allowing the diagnostic function to work in conjunction with the chip's layout diagram.

This enables precise identification of SRAM error locations within the chip and their root causes.

Event Review

START™ v5 and EZ-BIST™ v2 have also strengthened the SRAM clustering mechanism, which can be integrated with the chip's layout diagram to ensure proper timing requirements for placement and routing. For SRAM testing algorithms, START™ v5 and EZ-BIST™ v2 feature TEC 2.0 (Testing Element Change) that is designed based on iSTART-TEK's patented UDA (User Defined Algorithm) architecture.

TEC enables dynamic modification of SRAM test algorithms during the CP (Chip Probing) stage simply by changing tester commands, without requiring any modifications to the chip design. This makes DPPM (Defective Parts Per Million) control much more manageable.

The key advantage of TEC lies in the UDA patent, which allows modularization of SRAM testing algorithms—similar to stacking LEGO bricks. By recombining these modular components, new SRAM test algorithms can be generated. This enables chip developers to design customized SRAM test algorithms based on specific chip functions and applications, ultimately reducing DPPM rates.

iSTART-TEK's new products, START™ v5 and EZ-BIST™ v2, provide solutions for AI chips and automotive electronic chips, enhancing chip yield rates, reducing testing costs, and increasing market competitiveness.

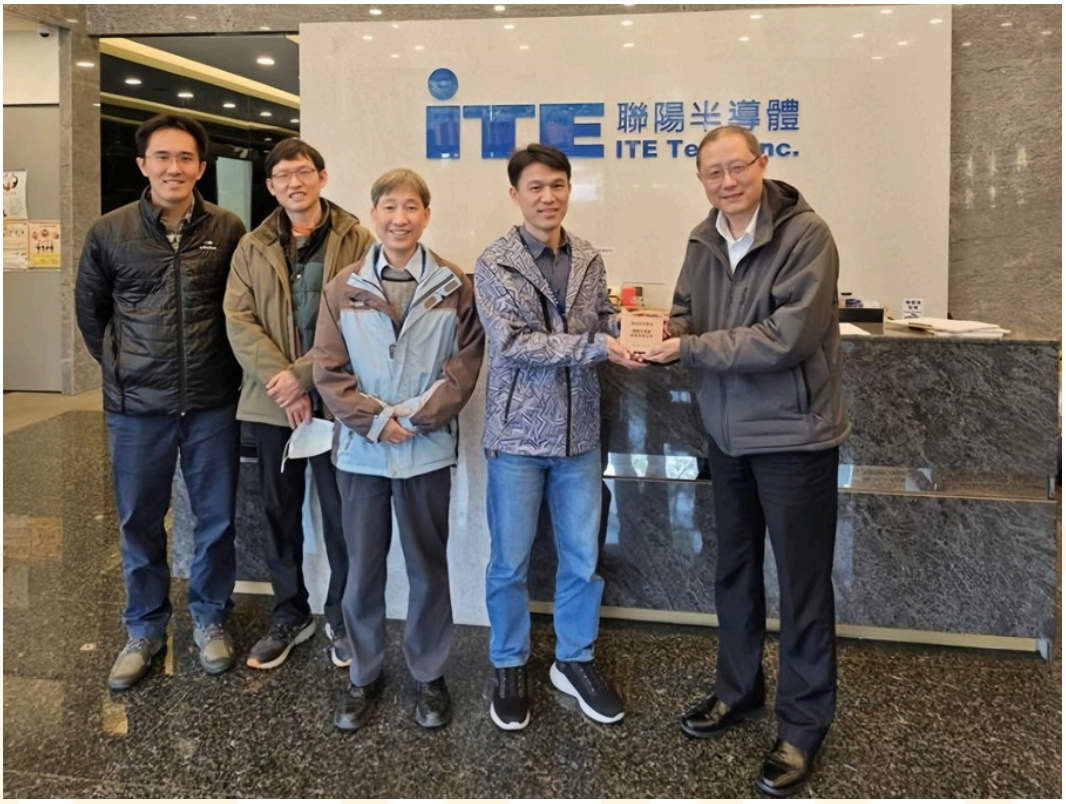
iSTART-TEK Appreciates the Support of Shanghai Automotive lC Engineering Center Co. Ltd.

The overall performance of START™ v5, iSTART-TEK's new product, has been enhanced by at least 50% compared to START™ v3. This new version strengthens SRAM repair technology, introduces CIM testing and repair capabilities, and integrates with the RISC-V technology. A major breakthrough in this release is the full-process DFT integration with third-party EDA tools.

Thanks to the support of Shanghai Automotive lC Engineering Center Co. Ltd. (SAICEC), START™ v5 has successfully achieved a complete DFT workflow design with third-party EDA tools.

iSTART-TEK's new product, START™ v5, enhances the yield of AI chips and automotive electronic chips, reduces chip testing costs, and boosts market competitiveness.

Gratitude to ITE Tech. Inc. for Long-Term Support of iSTART-TEK



ITE Tech. Inc. (ITE) is a professional fabless IC design house, established in 1996 and headquartered in Hsinchu Science Park. ITE started from the development of PC and NB Controller chips in the early years and takes the global lead in Super I/O as well as Keyboard and Embedded Controller technology.

ITE is one of iSTART-TEK's important partners. With ITE's continuous technical feedback and guidance, iSTART-TEK has been able to make consistent progress in product development. We sincerely thank ITE for its long-standing support and trust.

We Sincerely Appreciate HED for Its Long-Term Support of iSTART-TEK

CEC Huada Electronic Design Co., Ltd. (HED) is dedicated to the development of security SE chips, security MCU chips, and smart card IC, focusing on aspects such as applications in FinTech, network communication, IoT, Internet of Vehicle, smart mobility, and smart manufacturing.

HED is an important partner of iSTART-TEK. With the technical guidance and encouragement from HED, iSTART-TEK has been able to continuously improve in product development. We are grateful for HED's support and trust.

iSTART-TEK's EDA Tools and IP Recognized by Leading Chinese New Energy Vehicle Manufacturers

As the semiconductor industry competition between the U.S. and China extends to the automotive sector, China is actively promoting the enhancement of its domestic chip manufacturing capabilities. Currently, its domestically produced automotive chips account for 15% of usage and continue to grow. The annual revenue of the automotive chip industry exceeds USD 80 billion. Traditional fuel vehicles usually require more than 700 chips, while electric vehicles need more than twice that number.

iSTART-TEK's EDA tools have obtained ISO 26262 TCL1 certification and provide customized features including: Power-On Test (POT), Circuit Self-Verification (CSV) for SRAM testing circuits, Memory Status Watch-Dog (MSW) for identifying SRAM error signals, Automatic Repairing Flow (ARF) for SRAM, and Testing Element Change (TEC) for dynamic configuration of SRAM testing algorithms.

In addition, iSTART-TEK has launched eFlash BIST IP (eFlash Testing and Repair IP) to help automotive chip developers efficiently complete eFlash testing and repair tasks. It offers configurable test planning, shortens the development time of automotive chips, and reduces chip testing costs.

Foreign automotive chip suppliers are now facing a choice between expanding production in China or losing the market. Chinese car manufacturers are more inclined to purchase domestic chips, as it not only ensures supply chain stability but also enables closer collaboration with Chinese chip design companies.

iSTART-TEK, with its technological innovation, high yield, small area circuits and cost advantages, meets customer demands for improved chip quality and reduced testing costs.

Customers Mass-Produce Automotive and Consumer Chips with iSTART-TEK Solutions

On December 11, 2024, iSTART-TEK participated in the Shanghai IC 2024 Annual Industrial Development Forum & the 30th China IC Design Industry Exhibition (ICCAD-Expo) at Shanghai World Expo Exhibition & Convention Center, showcasing products that have been successfully mass-produced by customers using iSTART-TEK's solutions.

Automotive Electronics Series

iSTART-TEK's customers have applied the EDA tool START (SRAM Testing and Repair Circuit Development Environment) to automotive-related chips, including driver ICs, power management ICs, and high-performance automotive-grade safety ICs. The end products cover automotive instrument clusters, CIDs (Central Information Displays), HUDs (Head-Up Displays), C-V2X, smart cockpits, dash cams, and other vehicle devices.

Consumer Electronics Series

iSTART-TEK's EDA tools, START and EZ-BIST (SRAM Testing Circuit Development Environment), have also been applied to consumer product-related chips, including control ICs and IoT security authentication ICs. End products include laptops (Huawei, Lenovo, Google), domain controllers, monitors, and other consumer electronics.

iSTART-TEK's EDA tool START enhances chip yield through patented SRAM repair technology, while EZ-BIST meets the needs of consumer chips for DPPM control. Additionally, TEC (Testing Element Change), developed based on a patented architecture, allows chip developers to modify SRAM test algorithms after the CP stage via the JTAG interface, achieving optimal DPPM control.

Recently, iSTART-TEK's products have also been adopted in NPUs, and more AI-related chips are expected to utilize iSTART-TEK's memory testing and repair solutions in the future.

Integrating iSTART-TEK's EDA Tools with Other EDA Tools to Complete the Full DFT Flow

Key Advantages

- As SoC designs become increasingly complex, iSTART-TEK focuses on improving the SCAN technology within the DFT process, optimizing the overall workflow.
- SSN technology allows for parallel processing of the loading and reading steps of the SCAN Chain, eliminating the need to wait for the entire SCAN Chain to load before starting output.
- SSN typically divides the SCAN Chain into multiple segments or hierarchies, with each segment being independently controllable.
- The Insertion Bit mechanism determines which segment receives the test data.
- Parallel processing improves the overall SCAN Flow efficiency, reduces testing time, and dynamically configures to enhance SCAN Flow flexibility.
- Debugging capability is enhanced, allowing for more precise and quicker identification of problem locations.

Exciting Content

Completed DFT Flows (iSTART-TEK EDA Tools + SCAN + ATPG)

Reconfigurable Memory Test Algorithm Architecture

EZ-TEC (Testing Element Change)

The behavior of traditional algorithms cannot be modified if issues occur during Chip Probe (CP) and Final Test (FT) after chip tape-out. iSTART-TEK's Test Element Change (TEC) function, featuring a Graphical User Interface (GUI), modularizes algorithm behaviors, enabling easy rearrangement and the creation of new test algorithms. This enables dynamic adjustment and element rearrangement during CP and FT testing. Even if customers do not adopt iSTART-TEK's MBIST circuits, they can retain their original BIST architecture and insert the IP form into the original circuit, providing significant convenience and flexibility in application.

Strengths of EZ-TEC

- lCoexists with existing MBIST circuits.
- lDecouples existing SRAM testing algorithms from elements.
- lElement-based architecture testing algorithms significantly reduce area.
- lAllows easy modification of SRAM testing algorithms through the JTAG interface after completing the CP phases.

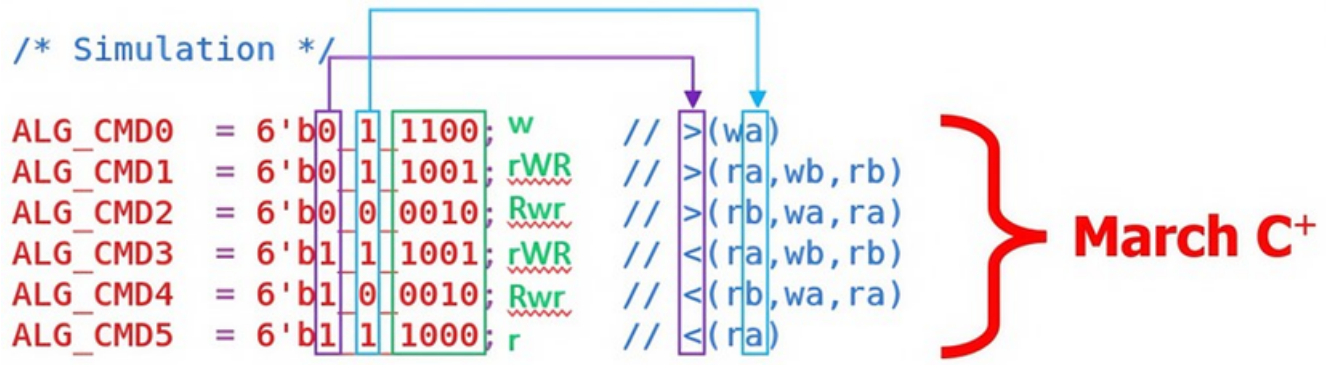
EZ-TEC Architecture

EZ-TEC can be independent with any MBIST EDA tools. Its modularized architecture facilitates the creation of highly cost-effective circuits, and can coexist with the existing memory testing circuits by being inserted beside the critical memory that is to be tested.

EZ-TEC can operate independently from any specific MBIST EDA tools. Its modularized architecture supports the construction of highly cost-effective circuits and can coexist with existing MBIST circuits by being inserted alongside critical memory that requires power-on testing. Here, SRAM_s indicates the original SRAM interface, while SRAM_t represents the SRAM interface processed by the MBIST. By multiplexing the control signals of SRAM, the original architecture is retained, and the new circuit is added in IP form, creating the SRAM_t interface. Finally, it connects to the top level through IEEE1500 or IEEE1149.1 interfaces. Circuit insertion must adhere to each respective clock domain, and once the clock domain is configured with EZ-TEC, the test elements can then connect to the designated SRAM.

Quickly Generate March C+ Algorithms with Elements

EZ-TEC is a modular architecture based on iSTART-TEK's U.S. patent, "METHOD FOR GENERATING A MEMORY BUILT-IN SELF-TEST ALGORITHM CIRCUIT." EZ-TEC allows users to adjust the sequence of algorithm elements during CP testing, such as the W, rWR, and Rwr elements shown in the figure below. Users only need to prepare four elements to combine and create a standard algorithm like March C+.



The Combination of Elements and Codes

Each element has a corresponding code, allowing users to create new testing algorithms by combining these codes.

```
parameter top_default_grp_id_width      = 1;
parameter top_default_meb_id_width      = 1;
parameter top_default_SEQ_STATE_WIDTH   = 2;
parameter top_default_RAM_SEQ_IDLE      = 2'd0;
parameter top_default_RAM_SEQ_PRE       = 2'd1;
parameter top_default_RAM_SEQ_APPLY     = 2'd2;
parameter top_default_RAM_SEQ_DONE      = 2'd3;
parameter top_default_SEQ_ADDR_WIDTH    = 10;
parameter top_default_action_width      = 4;
parameter Rwr                           = 4'b0010;
parameter r                             = 4'b1000;
parameter rWR                           = 4'b1001;
parameter w                             = 4'b1100;
```

Change Testing Algorithm Behaviors

Users can configure and modify testing algorithm behaviors through external interfaces, such as JTAG or send_command in the testbench.

send_command task

send_command = {PRL_ON, GRP_EN, MEB_ID, BG, ALG_CMD, MEN}

- PRL_ON：Determine to perform parallel testing.
- GRP_EN：Determine the group to be tested (each bit represents one group).
- MEB_ID：Determine the Memory ID to be tested (0 represents testing all memories).
- BG：Specify the background sequence for testing.

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- BG：Specify the background sequence for testing.

BG[1:0]	Pattern
00	0x0F → 0x5A
01	0x0F
10	0x5A
11	0x0F → 0x5A

- ALG_CMD = {ALG_CMD12, ALG_CMD11, … , ALG_CMD1, ALG_CMD0}
- MEN：Initiate the Memory BIST testing

ALG_CMD

- ALG_CMD0~12 = {direction, cmd_parity, action}
- direction：Specifies the order of address testing. 0 indicates ascending order, while 1 indicates descending order.
- cmd_parity：Determines the background for the first read/write operation of each element. 1 represents “a”, while 0 represents “b”.
- action：Obtains the value represented by each element from the MBIST code.

EZ-TEC Interface Pins

EZ-TEC supports IEEE1149.1 and IEEE1500 interfaces. The MCK (Memory BIST Clock) is the clock signal for MBIST, and RSTN (Memory BIST Reset) is the reset signal for MBIST.

Signal	Description
IEEE1149.1	
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode State
TRST	Test Reset
TCK	Test Clock
IEEE1500	
WSI	Wrapper Serial Input
WSO	Wrapper Serial Output
WRCK	Wrapper Serial Clock
WRSTN	Wrapper Reset
UpdateWR	Update Wrapper Register
ShiftWR	Shift Wrapper Register
SelectWIR	Select Wrapper Instruction Register
CaptureWR	Capture Wrapper Register

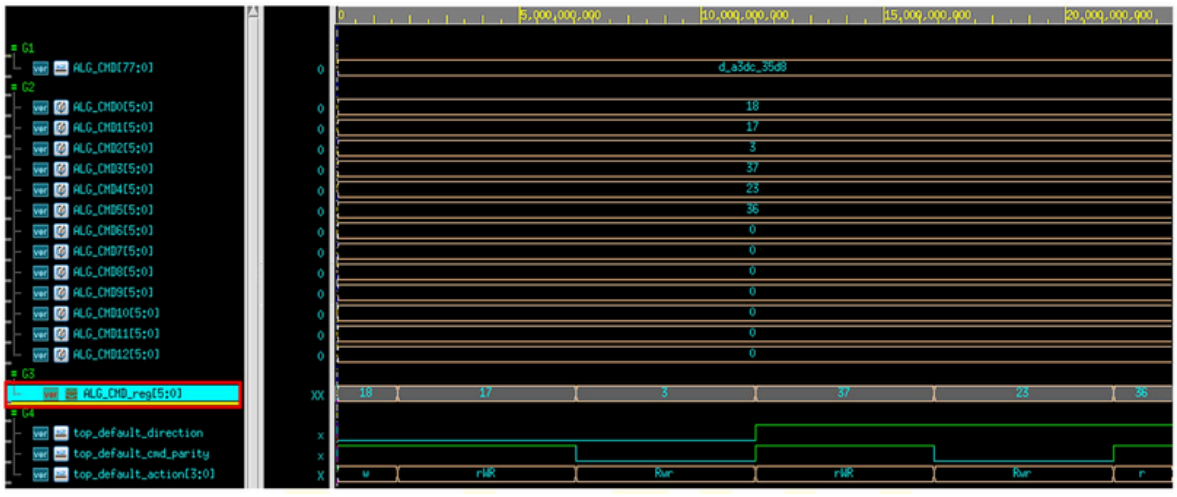
MBIST	
MCK	MBIST Clock
RSTN	MBIST Reset

The Corresponding Interfaces of Different SRAM Types

Signal	Description	Signal	Description
Signal Port SRAM (sram_sp_1024x32)		**Dual Port SRAM (sram_dp_1024x64)**	
CLK	Clock	CLKA	Clock A
A[9:0]	Address	CLKB	Clock B
D[5:0]	Data In	TAA[9:0]	Address A
CEN	Chip Enable	TAB[9:0]	Address B
WEN	Write Enable	TDA[63:0]	Data In A
Q[5:0]	Data Out	TDB[63:0]	Data In B
Two Port SRAM (rf_2p_24x28)		TCENA	Chip Enable A
CLKA	Clock A	TCENB	Chip Enable B
CLKB	Clock B	TWENA	Write Enable A
AA[4:0]	Address A	TWENB	Write Enable B
AB[4:0]	Address B	QA[63:0]	Data Out A
DB[27:0]	Data In B	QB[63:0]	Data Out B
CENA	Chip Enable A		
CENB	Chip Enable B		
QA[27:0]	Data Out A		

EZ-TEC Waveform

ALG_CMD collects the signals from 0 to 12. After shifting by 6 bits, the result is stored in ALG_CMD_reg, and the March C+ algorithm is then executed sequentially.



EZ-TEC Area Proportion

iSTART-TEK's EZ-TEC adopts the concept of Hardware Sharing, so as the number of SRAM units increases, the area growth rate becomes smaller.

Memory Instance	20	30	40	50
Area(um^2)	2410.379998	3282.678005	4158.378012	5021.226019
	1.42%	1.29%	1.22%	1.18%

library	tcbn28hpcplusbwp35p140ssg0p9vm40c_ccs
condition	MEM = 1024x32 = 8481.255250 um^2
frequency	MCK = 10MHz, TCK = 10MHz

After chip production, users can adjust algorithm behaviors through EZ-TEC at the CP testing stage. Whether without changing the original MBIST architecture or adopting other providers' MBIST solutions, iSTART-TEK's EZ-TEC IP can rearrange and develop new testing algorithms, thereby increasing chip yield and reducing DPPM.

Function	Change algorithms after CP
Algorithms	All algorithms of START
Interface	SRAM interface, JTAG
SRAM's types	SP、2P、DP
Configurable	Other functions of START